

2025-1-10

- iMS4 Controller Pro Firmware Version History

**Controller Pro revB (from Sept 2024 / sn243750 onwards)**

**FW v2-5-110**

Added support for new ImageFormat class (variable size Image data)

Allows-

- \* The number of RF Channels that are programmed by the Image
- \* The number of bytes used by: Frequency (range 1 - 4, default 2), Amplitude (range 1 - 2, default 1),
- \* Phase (range 1 - 3, default 2), Sync Data (range 1 - 2, default 2).
- \* Whether amplitude and phase are sent as part of the image (if not, they can still be programmed using the Compensation LUT)
- \* Whether Sync Digital data is included with the Image
- \* Whether Sync Analog data is included with the image, and whether 1 or 2 channels are sent
- \* Combining multiple channels in pairs using 1 Image channel
- \* Combining all RF channels using 1 image channel

**FW v2-5-107**

Added support for external outputting of the internally generated image trigger and clock when iMS configured for internal image trigger and clock.

**Controller Pro revA**

**FW v2-5-110**

Added support for new ImageFormat class (variable size Image data)

Allows-

- \* The number of RF Channels that are programmed by the Image
- \* The number of bytes used by: Frequency (range 1 - 4, default 2), Amplitude (range 1 - 2, default 1),
- \* Phase (range 1 - 3, default 2), Sync Data (range 1 - 2, default 2).
- \* Whether amplitude and phase are sent as part of the image (if not, they can still be programmed using the Compensation LUT)
- \* Whether Sync Digital data is included with the Image
- \* Whether Sync Analog data is included with the image, and whether 1 or 2 channels are sent
- \* Combining multiple channels in pairs using 1 Image channel
- \* Combining all RF channels using 1 image channel

**FW v2-4-98**

Added support for double edge clocking of FPI bus. This provides an increase in maximum Image Clock rate from ~2.7 to ~3.5MHz in X-Y deflector applications

**FW v2-3-85**

Fix problem with Tone mode not working when called within mixed mode sequences

**FW v2-3-83**

Firmware update to support different memory allocation for HSC Synthesiser builds and other minor updates:

- \* Attempt to reconnect Ethernet interrupt port repeatedly
- \* Fix the internal clock rate for very slow sequence clock playback (< 1.6kHz)
- \* Update SDK interface to support download of very large sequences split over multiple download buffers.
- \* Speed up sequence programming for short sequences by looking up image UUID on download, not on usage.
- \* Improve interrupt context locking to protect shared access to sequence hardware
- \* Sequence DMA data checked in hardware for access type to prevent double programming of synthesiser registers resulting in RF corruption

**FW v2-2-79**

- \* Fix problem with erroneous preload of the image clock pre-scaler.

[A pre-scaler is applied for image clock rates below 1.5KHz.

Minimum clock rate = 15.3Hz. Clock rates below 15.3Hz are now F/W limited to 15.3Hz]

**FW v2-2-78**

- \* Fix problem preventing the download of many sequences ( $\sim 10^5$ )

**FW v2-2-77**

- \* Fix problem with playing large Images with >12,600 points.

[After fix, maximum = 1.25 million points per single image]

**FW v2-2-76**

- \* Fix problem causing the first image point in a sequence playback to be randomly missed when using external clock & trigger.

**FW v2-2-75**

- \* Fix sequence problem which caused firmware to crash when a queue contained a single sequence in recycle or stop-recycle mode.
- \* Fix sequence problem which caused iMS to hang when playing large numbers of short images with many repeats.
- \* Fix USB FIFO overflow detection error.